In the Claims:

Please amend claims 1-3, and add new claims 4-7 as indicated below. This listing of claims replaces all prior versions.

1. (Currently Amended) A multi-issue processor comprising:

a register file; and

[[-]] a plurality of issue slots, each one of the plurality of issue slots ~~comprising~~ including

a plurality of functional units,

an input routing network that provides multiple data path outputs for a single data path input, the input routing network receiving data from the register file on the single data path input via a single data input path and providing data from the register file to functional units of the plurality of functional units, the data provided on the multiple data path outputs via multiple data output paths, and

a plurality of holdable registers that hold duplicate data from the register file, ~~the plurality of issue slots comprising~~

wherein in a first set of the plurality of issue slots the holdable registers store data on the multiple data output paths of the first set and in a second set of the plurality of issue slots the holdable registers store data on the single data input path corresponding to the input routing networks of the second set. ~~; and~~

~~a register file, separate from the plurality of holdable registers, accessible by the plurality of issue slots;~~

~~wherein a location of at least a part of the plurality of holdable registers in the first set of issue slots is different in relation to the functional units of the respective issue slots from a location of at least a corresponding part of the plurality of holdable registers in the second set of issue slots.~~

2. (Currently Amended) A multi-issue processor according to Claim 1, wherein[[:]]

[[-]] a first instruction set accesses at least the first set of issue slots; and

[[-]] a second instruction set accesses the second set of issue slots.

3. (Currently Amended) A multi-issue processor according to Claim 1, wherein[[:]]

the input routing network of each of the plurality of issue slot has a plurality of data path inputs; and

in the ~~first~~ second set of issue slots ~~the location of~~ holdable registers of the plurality of holdable ~~data~~ registers are located between each of the inputs of the input routing network and the register file. ~~is at individual data inputs of the functional units, while in the second set of issue slots the location of the plurality of holdable data registers is at common data inputs of the functional units.~~

4. (New) A multi-issue processor according to Claim 1, wherein, in the first set of issue slots, holdable registers are located between the input routing networks and each of the plurality of function units.

5. (New) A multi-issue processor according to Claim 1, wherein the first set of issue slots are accessed by a first set of instructions for a very-large-instruction-word (VLIW) processor and the second set of issue slots are accessed by a second set of instructions that are used by an interrupt routine.

6. (New) A multi-issue processor according to Claim 5, wherein the second set of instructions has less instructions than the first set of instructions.

7. (New) A multi-issue processor according to Claim 1, wherein the first set of issue slots has more issue slots than the second set of issue slots.